# AZ473 [JTAG ADAPTER] Instruction Manual

DTS INSIGHT CORPORATION.

AZ473: JTAG ADAPTER

Instruction Manual

No. M2381YL-03

# **Publication History**

Edition	Date of Issue	Description
First Edition	June 15, 2009	Initial publication
Second Edition	April 9, 2012	Another name is added to the TVccd signal
Third Edition	October 18,2015	Addition of EU directives

- (1) No part of this manual may be reproduced or transmitted in any form or by any means, electronic or mechanical, without the written permission of DTS INSIGHT CORPORATION.
- (2) The contents of this manual are subject to change without prior notice due to improvement of the functionality.
- (3) If any question about the contents of this manual arises, contact DTS INSIGHT CORPORATION.
- (4) DTS INSIGHT CORPORATION shall not be held responsible for direct or indirect adverse effects resulting from operation of this system irrespective of the preceding item (3).

Product and company names mentioned in this manual are the trademarks of their respective owners.

© 2009 DTS INSIGHT CORPORATION. All rights reserved

Printed in Japan

# Contents

1	Overview	3
1.1	External configuration & dimensions of the Adapter area	3
1.2	Setup Pull-up Register on /TRES Signal	4
1.3	Target Probe	5
2	Target Interface	6
2.1	Signal and pin assignment	6
2.2	Circuit Specification	7
2.3	Pin assignment of the target side	10
3	DC Characteristics	11
4	AC Characteristics	12
4.1	Clock Timing	12
4.2	Signal Timing (as seen from the adapter side)	12
4.2.1	A target system which TDO is output on the falling edge of TCK	12
4.2.2	A target system which TDO is output on the rising edge of TCK	13
5	Connecting AZ473 and a Target System	14
6	EU Directive	16
6.1	CE marking	16
6.2	WEEE marking	16

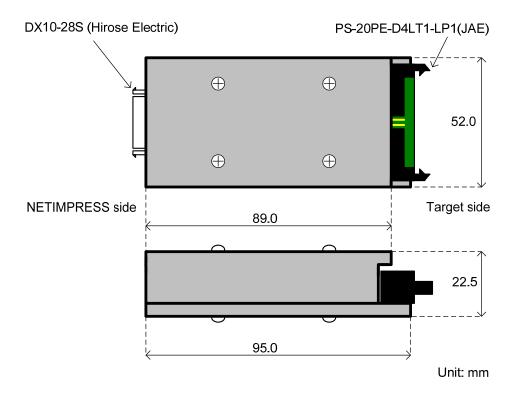
## 1 Overview

AZ473 JTAG adapter converts the standard signal output by the flash microcomputer programmer NET IMPRESS series to the JTAG signal

AZ473 supports programming flash ROM of a microcomputer on a user system using JTAG protocol.

# 1.1 External configuration & dimensions of the Adapter area

The figure below illustrates external configuration and dimensions of the adapter area of AZ473.



## 1.2 Setup Pull-up Register on /TRES Signal

This adapter has a DIP switch which you can use to switch whether pulling up or not /TRES output to +XV power supply.

(See the chapter 2. Target Interface for detail of /TRES output and +XV power supply.)

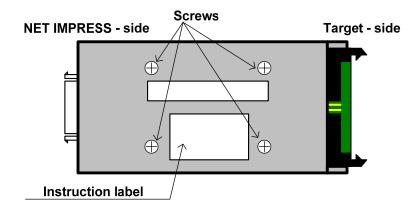
The figure below illustrates overall external configuration and dimensions of AZ473.

#### /TRES output is pulled up in factory default.

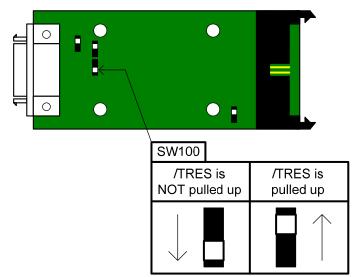
Be sure to setup this adapter for signal state of a target system before using.

#### [How to open the case]

Remove the screws and open the upper case.



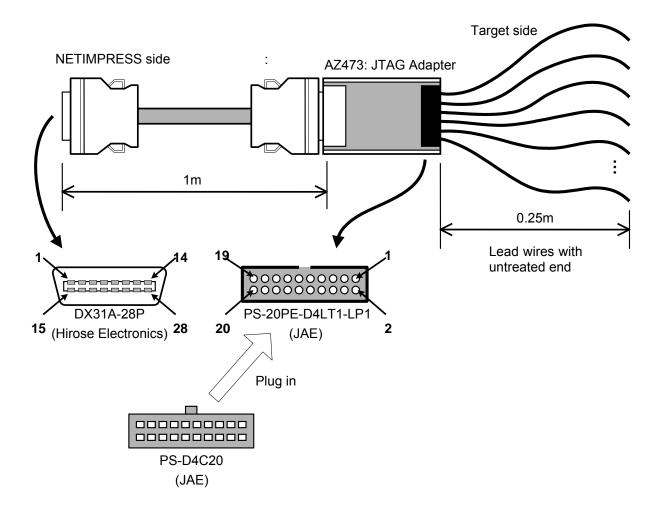
#### [Location and position of the DIP switch]



- \* Be sure to power off NETIMPRESS and a target system when changing the setting.
- \* Do not change the state of switches other than the SW100 switch.
- \* Replace and secure the upper case with screws after changing the switch setting.

# 1.3 Target Probe

Pin layout of each connector is numbered as viewed from the mating side.



# 2 Target Interface

# 2.1 Signal and pin assignment

The table below lists signals of AZ473 at user target side.

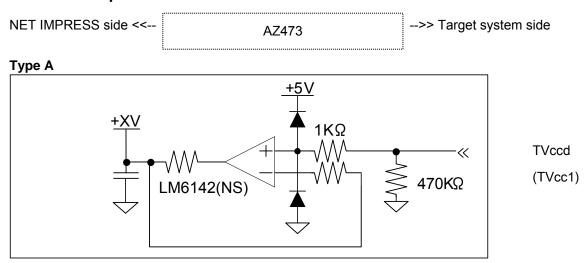
I/O (Input and Output) information is for AZ473.

Signal Name	Definition		Туре
TVPP1	TVPP1 output from NETIMPRESS  (Output terminal to target microcomputer for programming voltage. It may not be necessary depending on microcomputer.)		L
VCC	VCC output from NETIMPRESS (+ 5V fixed, maximum 30 mA)	0	_
TVccd (TVcc1)	Power input from user target to AZ473 Used as buffer power source for I/O signals of AZ473	I	А
TCK	JTAG TCK output	0	С
TDI	JTAG data output	0	В
TDO	JTAG data input	I	Н
TMS	JTAG TMS output		С
/TRES	Hardware reset output		J
/TICS0	/TICS output from NET IMPRESS (+ 5V output)	0	К
/TICS1	/TICS output from NET IMPRESS, which is converted to the voltage level of TVccd(TVcc1) by buffer in AZ473		D
WDT	WDT output from NET IMPRESS, which is converted to the voltage level of TVccd(TVcc1)	0	I
TAUX3	JTAG nTRES output	0	F
TAUX4	Reserved output terminal. Connect as needed only.		F
TMODE	Reserved output terminal. Connect as needed only.	0	Е
Reserved	Reserved terminal. Do not connect any signal at target side.	_	_
GND	Connect with GND at target side.	_	_

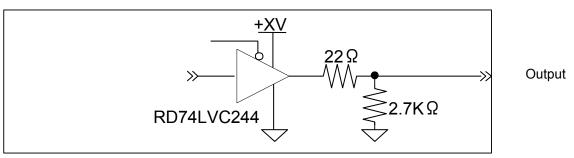
For details of the standard I/O signals of NET IMPRESS series, see the NET IMPRESS Instruction Manual.

Definitions of signals may vary depending on Control Modules. See the instruction manual for the Control module for details.

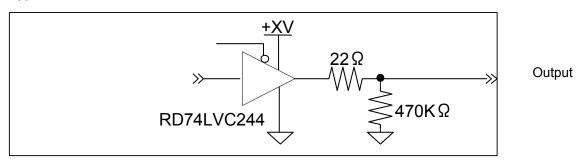
# 2.2 Circuit Specification



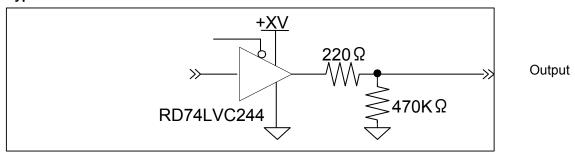
## Type B



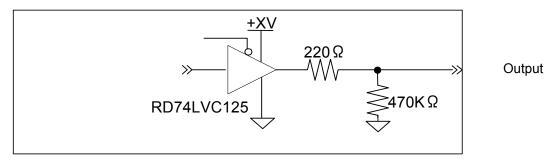
Type C



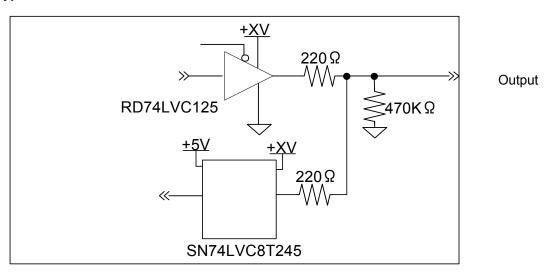
Type D



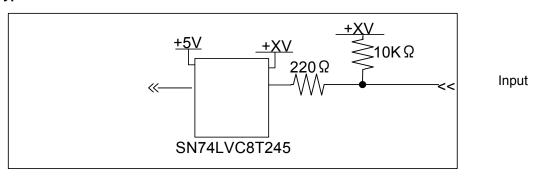
Type E



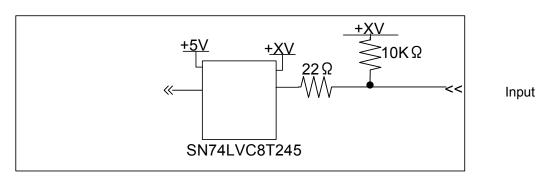
Type F



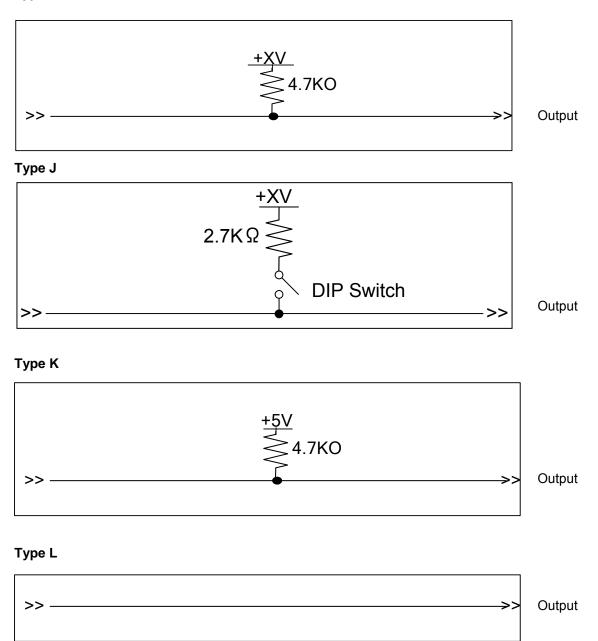
Type G



Type H



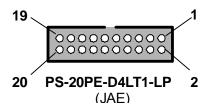
#### Type I



- $^{*}$  When TAUX3, TAUX4, and TMODE are pulled up on the target system, resistances less than 10 K $\Omega$  are recommended.
- \* +XV can be used as an interface power supply to equal the signal level with target system.
- \* VCC, TVPP1, /TICS0, WDT, /TRES are output from NETIMPRESS through AZ473 as it is without conversion. (/TICS0, WDT, and /TRES are pulled up in AZ473. For the output circuit, please refer to the instruction manual of NETIMPRESS.

# 2.3 Pin assignment of the target side

The table below lists pin assignment of the connector of AZ473 at the target side.



Pin No.	Lead Color	NET IMPRESS Signal Name I/O	
1	Brown	TVpp1	0
2	Red	Vcc	0
3	Orange	TMODE	0
4	Yellow	TVccd(TVcc1)	I
5	Green	GND	-
6	Blue	TCK	0
7	Violet	GND	-
8	Gray	TDI	0
9	White	GND	-
10	White & Black	TDO	I
11	White & Brown	TMS	0
12	White & Red	/TRES	0
13	White & Orange	/TICS0	0
14	White & Yellow	/TICS1	0
15	White & Green	WDT	0
16	White & Blue	TAUX3	I/O
17	White & Violet	TAUX4	I/O
18	White & Gray	Reserved	-
19	Light blue	/TSEQ	1
20	Yellow & Green	GND	-

<sup>\*</sup> I/O listed in the table above indicates input and output from the adapter to a target system.

<sup>\*</sup> The above listed GNDs (5, 7, 9, and 20) are common with each other in the adapter. Connect as many GNDs as possible to a target system for stable electric connection.

<sup>\*</sup> Be sure that untreated signal wires at the target side do not short out with other signal wires or metal parts of test pins, for example.

# 3 DC Characteristics

Listed +XV below are power supply voltage for I/O buffer, which are generated from TVccd(TVcc1).

Output voltages vary affected by voltage drop by serial resistances in the adapter and input circuit on a target system.

Signal	Item				Min	Max	Unit
TVccd	Input voltage	Vin		Absolute rating	-0.3	5.25	V
				Operate range	2.0	5.0	
	Input current	lin		_	_	526	nA
TCK	Output voltage	VoH	IoH = ±100 uA	_	+XV -0.2	_	V
TMS		VoL		_	_	0.2	
TDI	Output current	lout		+XV = 3.0 V	_	± 24	mA
				+XV = 5.0 V	_	± 24	
TDO	Input voltage	ViH		+XV = 3.0 V	2.0	_	V
				+XV = 4.5 V	3.15	_	
		ViL		+XV = 3.0 V	_	0.8	
				+XV = 4.5 V	_	1.35	
	Input current	lin		_	_	15	uA
/TRES *1	Output voltage	VoH		_	_	+XV	V

<sup>\*1</sup> Open collector output from NETIMPRESS is pulled up to +XV in the adapter.

For the specification of /TRES, refer to the instruction manual of NETIMPRESS.

## 4 AC Characteristics

## 4.1 Clock Timing

Signal name	Item	Min Max		Unit
TCK	At the time of data transmission	500K	5.0M	Hz
ICK	At the time of state transition		1.5625M	Hz

## 4.2 Signal Timing (as seen from the adapter side)

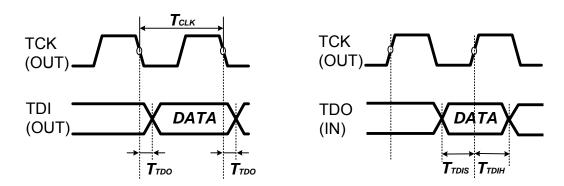
This section describes AC timings under conditions below.

TVccd(TVcc1) input (Voltage of target system): 3.0 V

Cable between NETIMPRESS and AZ473: AZ410 (1 m) \*Our standard

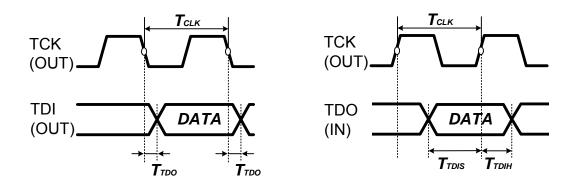
Cable between AZ473 and a target system: 0.25 m long untreated wires \*Our standard

# 4.2.1 A target system which TDO is output on the falling edge of TCK



Symbol	Item	Characteristic	Condition
T <sub>TDO</sub>	Delay time from the falling edge of TCK to TDI output	Max. 10 ns	Independent on JTAG clock frequency
T <sub>CLK</sub>	TCK cycle time	Min. 200 ns	JTCK = 5 MHz
T <sub>TDIS</sub>	Setup time for TDO to the rising edge of TCK	Min. 55 ns	Independent on JTAG clock frequency
T <sub>TDIH</sub>	TDO hold time after the rising edge of TCK	Min. 0 ns	Independent on JTAG clock frequency

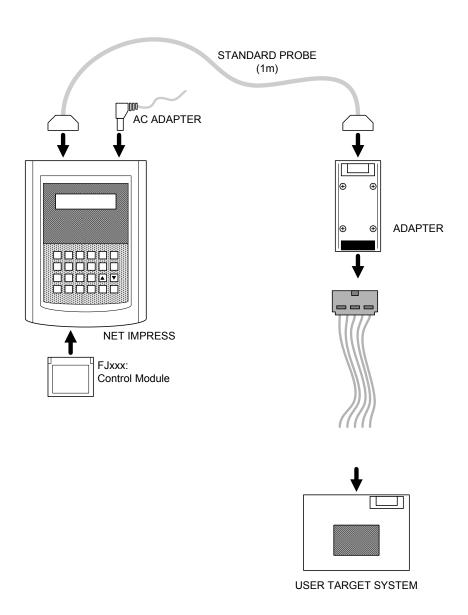
# 4.2.2 A target system which TDO is output on the rising edge of TCK



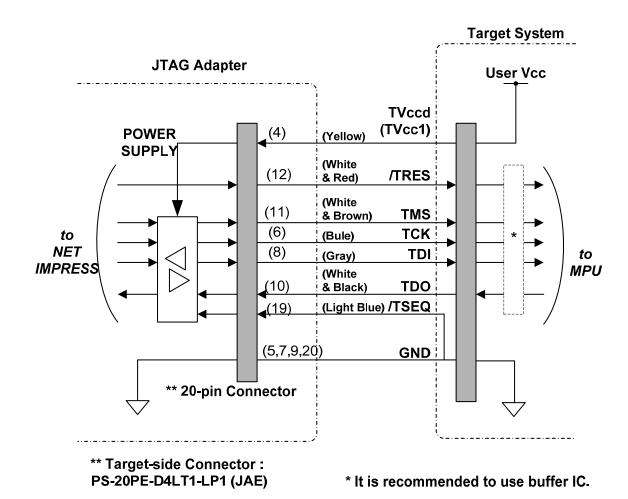
Symbol	Item	Characteristic	Condition
T <sub>TDO</sub>	Delay time from the falling edge of TCK to TDI output	Max. 10 ns	Independent on JTAG clock frequency
T <sub>CLK</sub>	TCK cycle time	Min. 200 ns	TCK = 5 MHz
T <sub>TDIS</sub>	Setup time for TDO to the rising edge of TCK	Min. 97 ns	Independent on JTAG clock frequency
T <sub>TDIH</sub>	TDO hold time after the rising edge of TCK	Min. 0 ns	Independent on JTAG clock frequency

# 5 Connecting AZ473 and a Target System

The figure below illustrates how NET IMPRESS, AZ473 and a user target system are connected.



The figure below illustrates the example of connection on a circuit.



/TSEQ can be connected to a target system only when the target system has security feature. Connect /TSEQ with GND of the target system when it has security feature. If it does not have security feature, leave /TSEQ open.

The numbers in parentheses are the pin numbers of the connector PS-20PE-D4LT1-LP1.

In this adapter, power supply (+XV) is generated from TVccd(TVcc1) to equal signal level with a target system.

See the NETIMPRESS Instruction Manual when connecting NETIMPRESS' original signals other than signals commonly used in JTAG communication.

For the signal lines not used, you can leave them open unless otherwise specified in the Control Module Instruction Manual.

#### 6 **EU Directive**

#### 6.1 **CE** marking

Item	Compliant standards
CE Marking	[EMC Directive]
*1	Emissions :EN61326-1 Class A
	Immunity: EN61326-1 Table 2(For use in industrial locations)
	[RoHS Directive]
	EN50581:2012

<sup>\*1</sup> The product in which CE Marking is indicated on the product serial label is an target.



This instrument is a Class A product, and it is designed for use in the **CAUTION** industrial environment. Please use this instrument in the industrial environment only.

#### 6.2 **WEEE marking**

#### WASTE ELECTRICAL AND ELECTRONIC EQUIPMENT DIRECTIVE (2012/19/EC)

(Waste Electrical and Electronic Equipment Directive (WEEE) is for EU countries)



AZ473 JTAG Adapter complies with WEEE Directive (2012/19/EC). Electric/electronic products carrying this mark must be disposed of separately from normal household wastes.

#### Product category:

With reference to the equipment types in the WEEE directive Annex 1, this product is classified as a "Monitoring and Control instrumentation" product. When disposing products in the EU, contact your local distributor. Do not dispose in domestic household waste.