DTS INSIGHT

STM32Fxxx Internal Flash Memory Instructions Manual

DTS INSIGHT CORPORATION

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Revision History

Edition	Date of issue	Description
1st Edition	May. 31, 2012	• Initial publication
2nd Edition	Jul. 31, 2012	• Description for STM32F2/F4Flash Software break is added.
3rd Edition	Sep. 30, 2012	• Description for STM32F0 is added.
4th Edition	Dec. 10, 2013	• Description for advice LUNA II is added. • Errata are corrected

Contents

1 Introduction

This is a brief manual for writing to Internal flash memory.

For details of ICE operating instructions, see the microVIEW-PLUS User's Manual (Common Edition) and microVIEW-PLUS User's Manual (MPU-Specific Edition).

2 Supported Install kit CD Versions

Device Model	Supported Versions		
	H2X600IK	SLX600	ZX600
STM32F1	1.01 or later	1.00 or later	3.10 or later
STM32F2/F4	1.01 or later	2.13 or later*	--
STM32F0	1.01 or later	2.16 or later	--

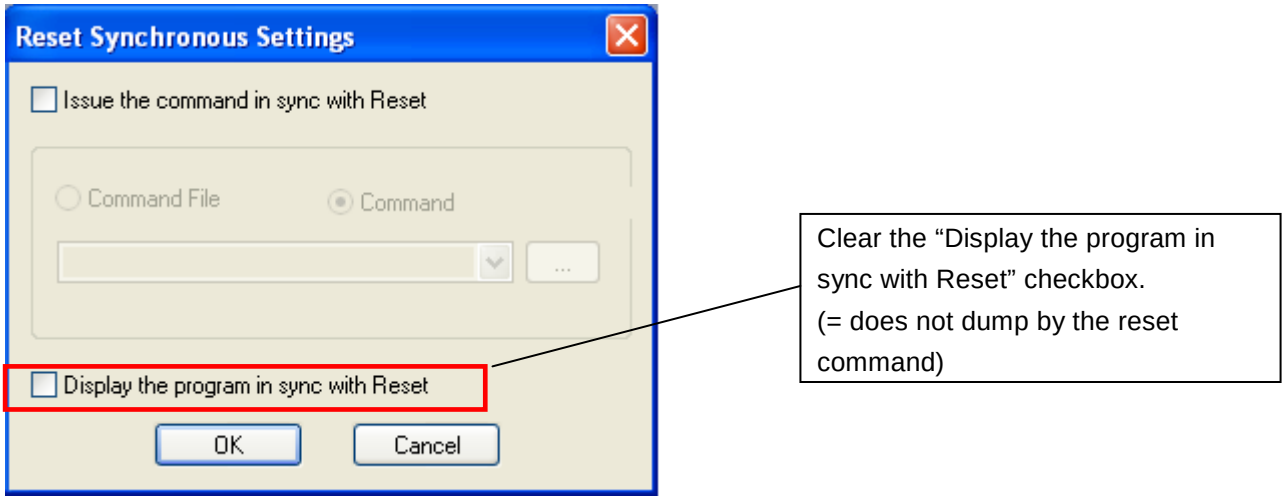
* For Flash software break, SLX600 Rev 2.14 or later is necessary.

3 Advance Preparation

3.1 If Nothing is Recorded on the Built-in Flash Memory

microVIEW-PLUS dumps a reset vector area to display a program (disassemble display) after connecting by reset commands. In case you are using Cortex-M series cores and nothing is recorded in the built-in flash memory (a vector table is 0xFFFFFFFF), 0xFFFFFFFE will be dumped and “ICE Error No.f58: Sticky error” may occur.

[Provision]
Right-click the Reset button on the toolbar, and then open the Reset Synchronous Setting dialog box.



After downloading the program to the built-in flash memory (correct vector table values are written), select this checkbox again.

3.2 MPU-specific Debug Control Register

In some cases, Cortex-M series core has a debug control register outside of the core. In this case, start debugging after setting the debug specific control register.

(MPU → MPU-Specific Setting → Synchronous memory operation)

Without settings, you may not be able to perform debug operation successfully.

The followings are setting examples.

*** Modify the settings as required.**

*** For details, see technical reference manuals for each MPU.**

1. Setup example for STM32F0xxx.

Settings

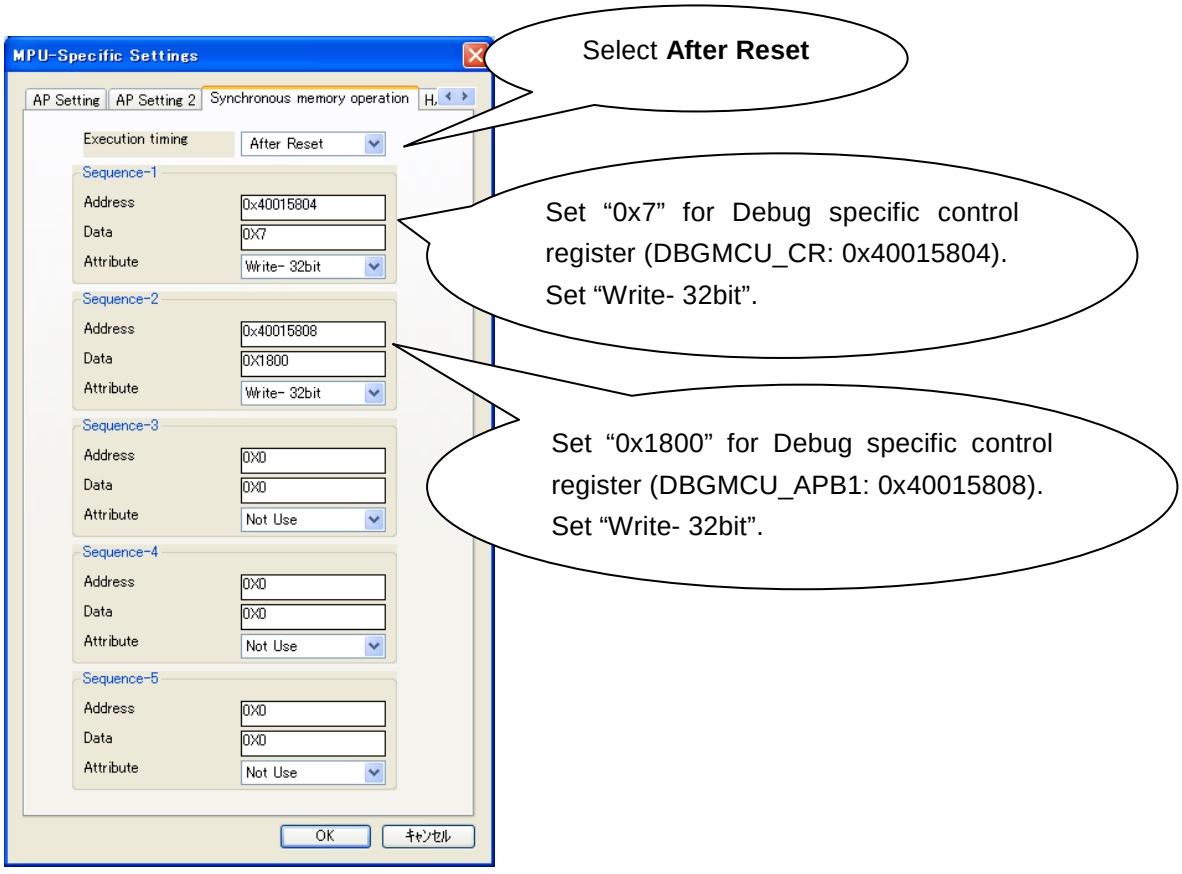
DBG_STANDBY=1: Debug Standby mode.

DBG_STOP=1: Debug Stop mode.

DBG_SLEEP=1: Debug Sleep mode.

DBG_IWDG_STOP=1: Debug independent watchdog stopped when core is halted.

DBG_WWDG_STOP=1: Debug Window Watchdog stopped when Core is halted.



2. Setup example for STM32F1xxx.

Settings

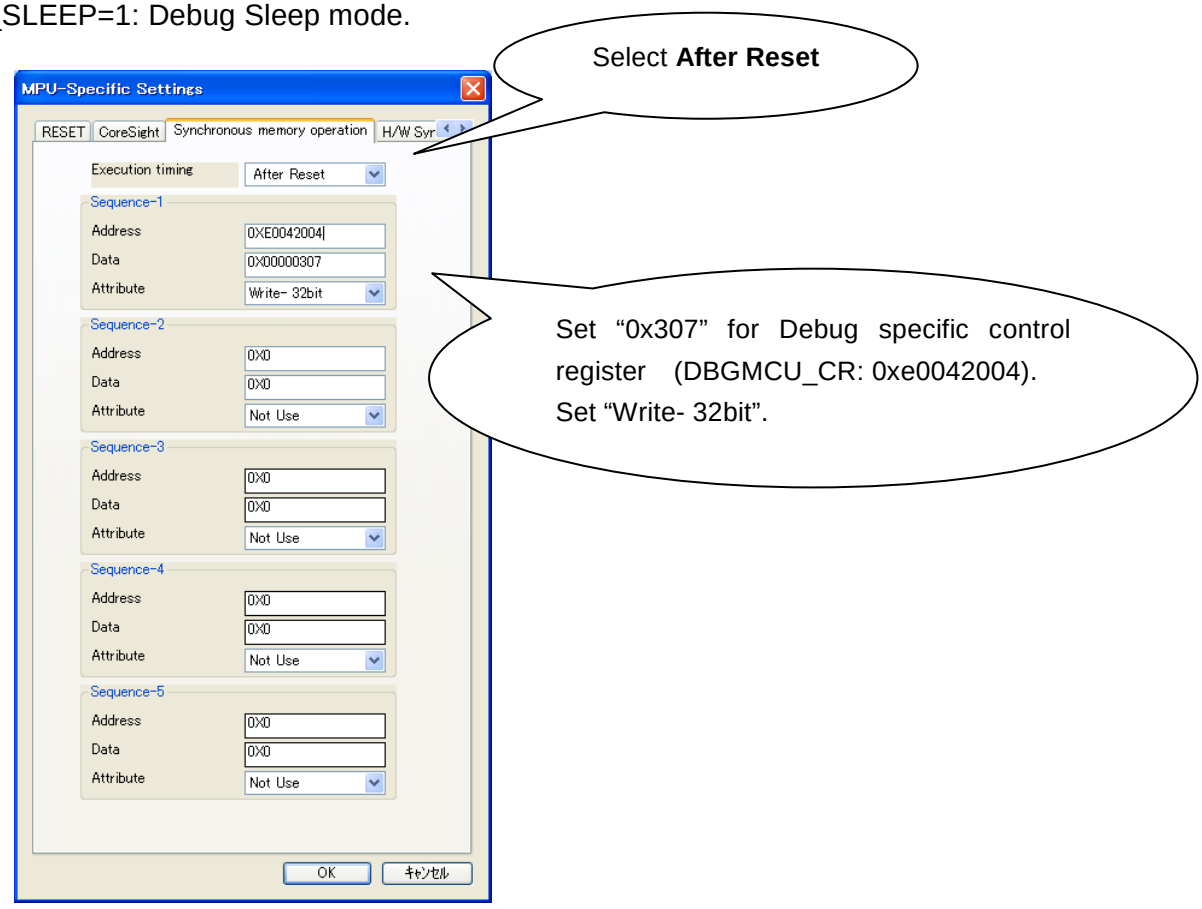
DBG_IWDG_STOP=1: Debug independent watchdog stopped when core is halted.

DBG_WWDG_STOP=1: Debug Window Watchdog stopped when Core is halted.

DBG_STANDBY=1: Debug Standby mode.

DBG_STOP=1: Debug Stop mode.

DBG_SLEEP=1: Debug Sleep mode.



3. Setup example for STM32F2xxx/ STM32F4xxx.

Settings

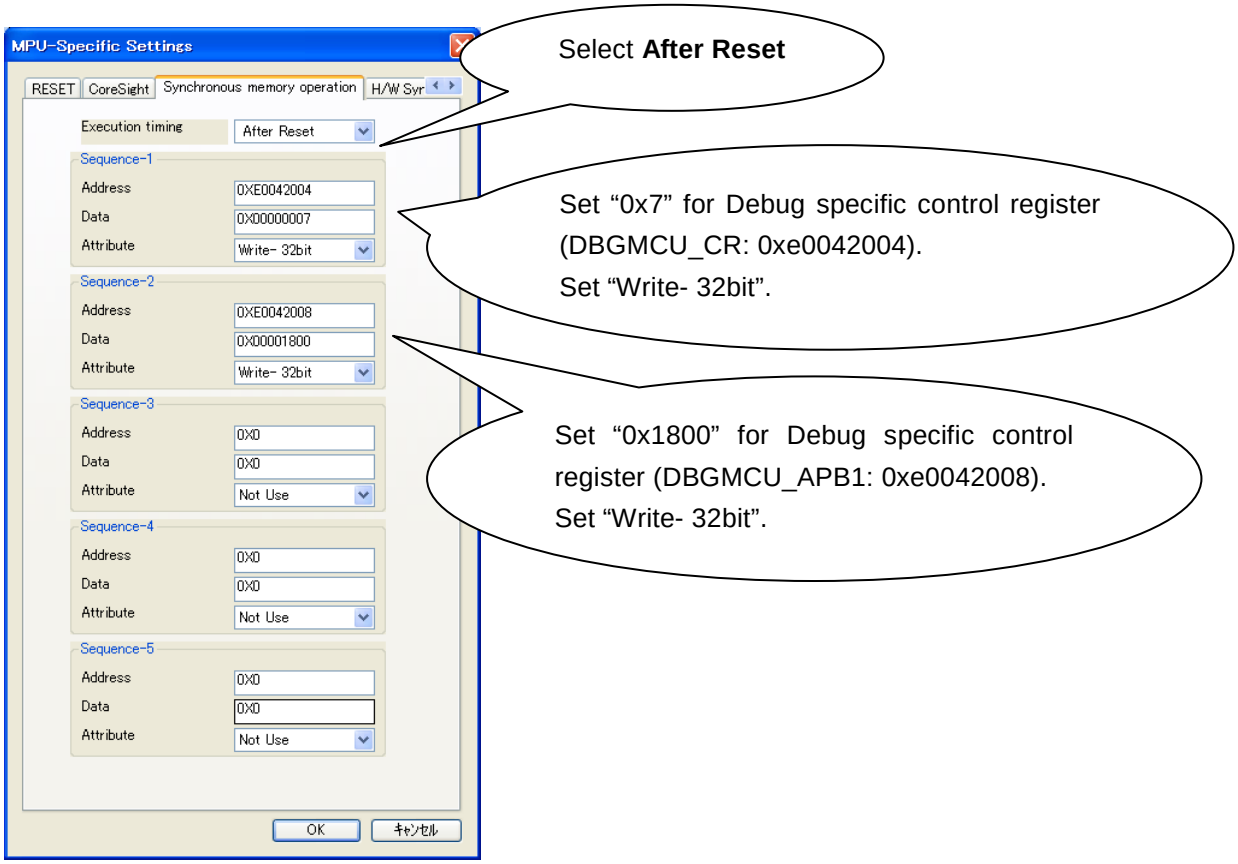
DBG_STANDBY=1: Debug Standby mode.

DBG_STOP=1: Debug Stop mode.

DBG_SLEEP=1: Debug Sleep mode.

DBG_IWDG_STOP=1: Debug independent watchdog stopped when core is halted.

DBG_WWDG_STOP=1: Debug Window Watchdog stopped when Core is halted.

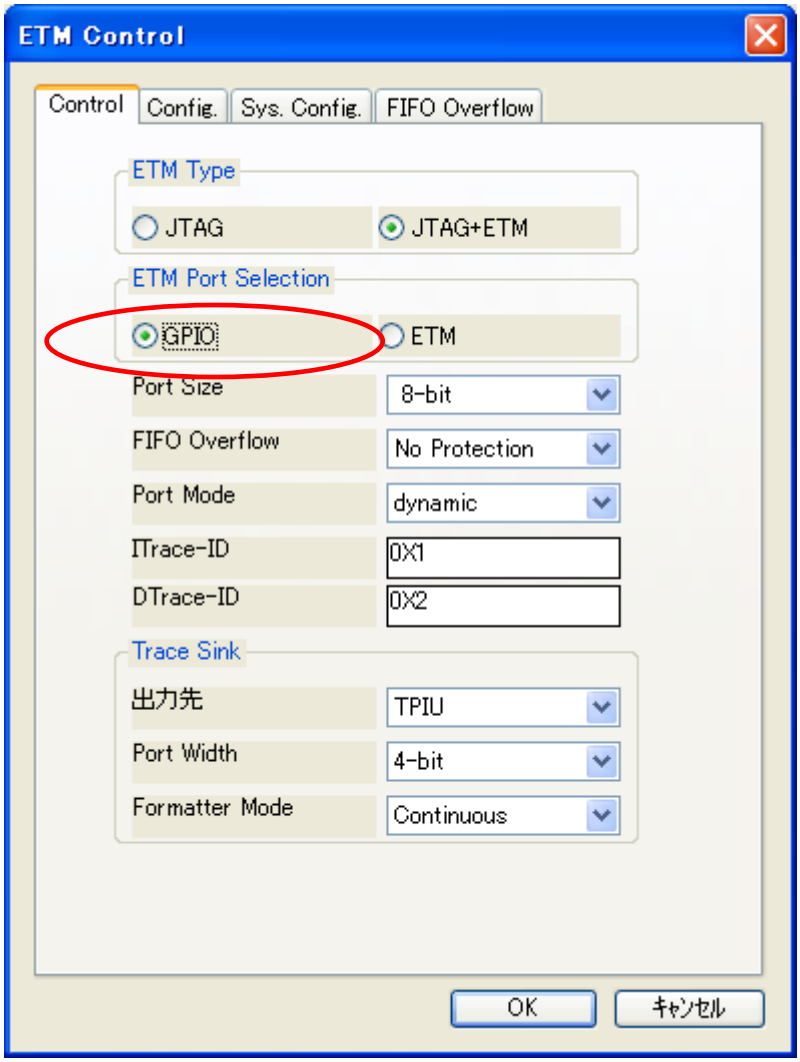


3.3 Settings for when ETM is disabled

When “ETM Type” setting is “JTAG”, this setting is unnecessary.

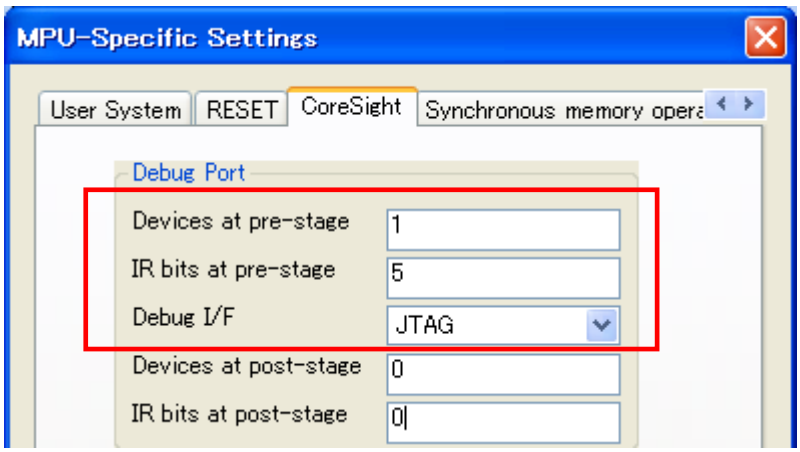
When the ETM setting of the board is invalid, please set “GPIO” for “ETM Port Selection”.

MPU → ETM Control



3.4 Changing I/F to connect

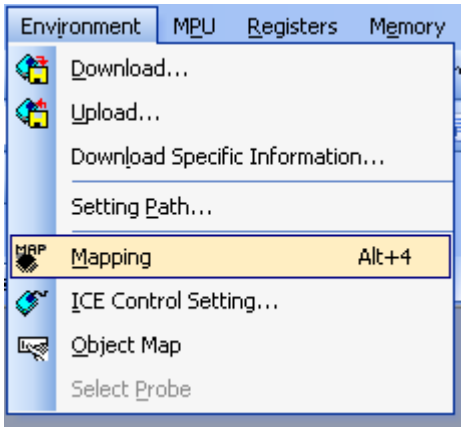
In case the debugger operation in SWD is unstable, switch it to JTAG I/F. Set the number of bypass TAP at pre-stage and the number of IR register bit at pre-stage then.



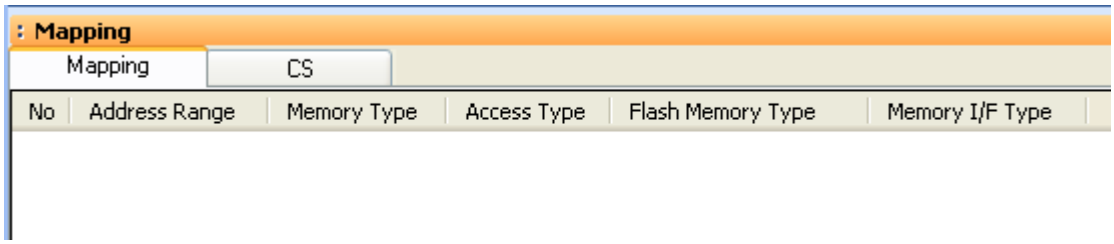
4 Setting the Memory Mapping

4.1 Setting up Flash Memory Mapping

Open the memory mapping window by clicking **Environments** – **Mapping**.

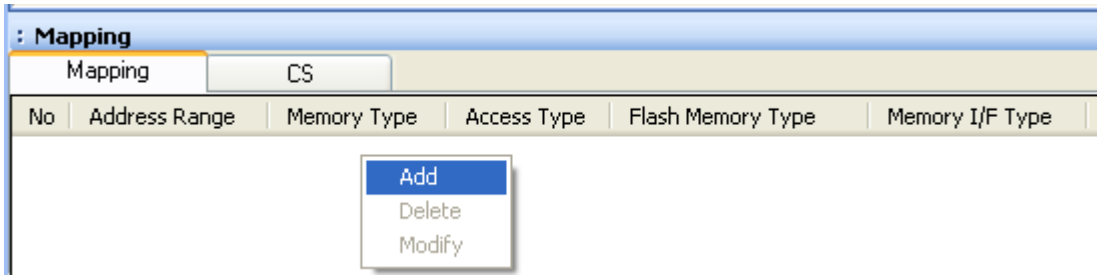


Memory map window as below is opened.

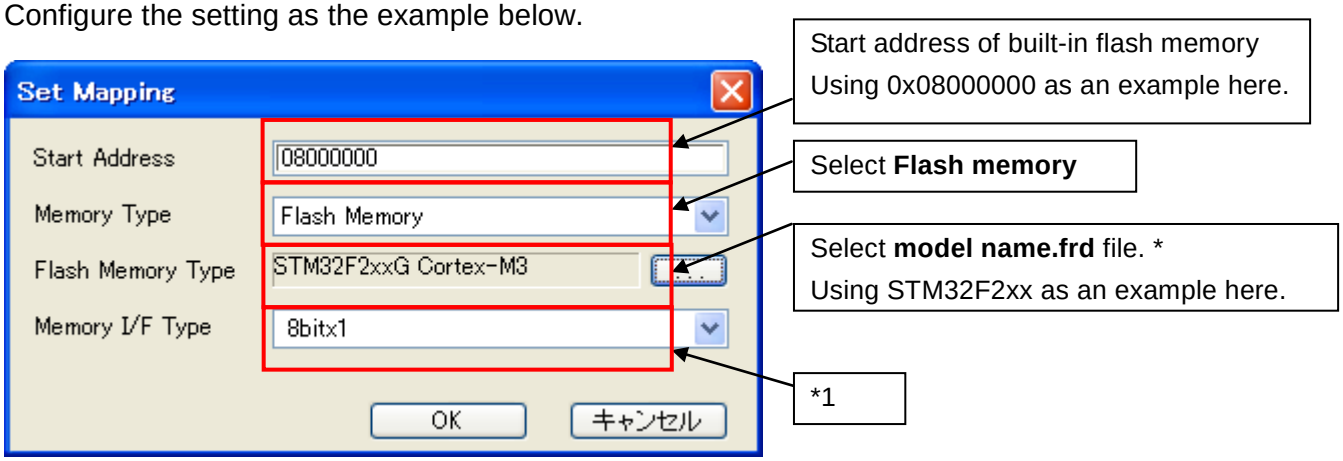


Set the mapping.

Right-click on the memory mapping window, and then select **Add**.



Configure the setting as the example below.



*1 Set as follows:

MPU	Setting value
STM32F0/F1	16bit×1
STM32F2/F4	8bit×1 *2

***2 Default configuration is 8bitx1. If the behavior like flash software break is slow, depending on the environment of user system, you can make it faster by changing the settings. For details, see Section 7.1.1 "If the Debugger behavior is Slow when using a Flash Software Break".**

4.2 Setting up User RAM for ICE

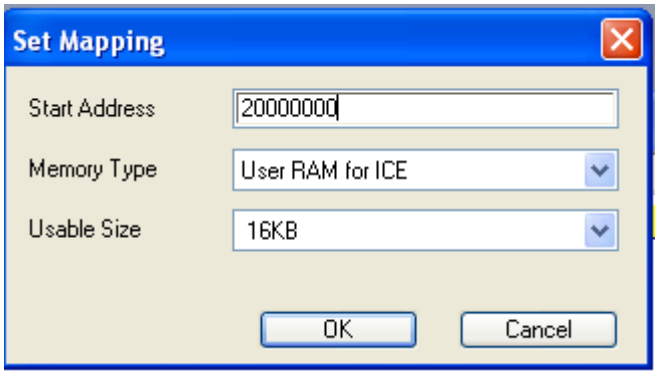
You can increase a download speed for flash memory by mapping a user RAM for ICE.

You can download to flash memory without the mapping setting though.

For User RAM for ICE, specify an area where ICE can occupy.

The following example is for when setting 16KB from 0x20000000.

For the actual settings, refer to the MPU memory map of yours.



5 Download to Flash Memory

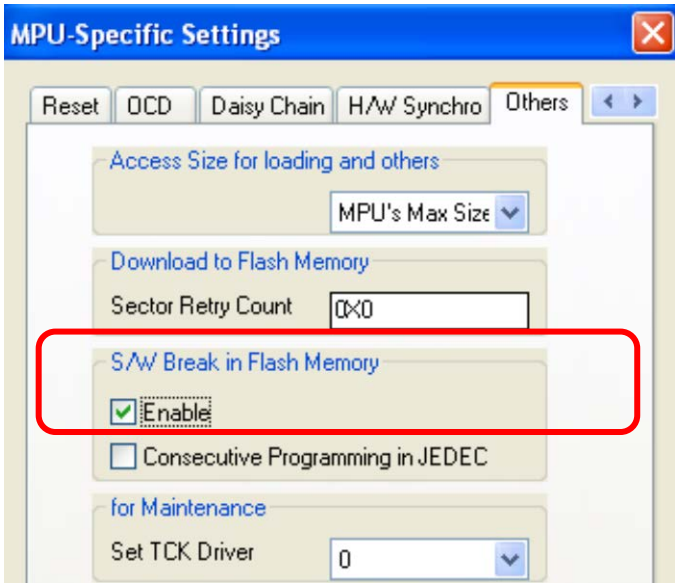
For details, see the microVIEW-PLUS User's Manual (MPU-Specific Edition).
Details of memory mapping settings are described on this manual. Please refer to the microVIEW-PLUS User's Manual (MPU-Specific Edition) for other contents.

6 Software Break in Flash Memory

For details, see the microVIEW-PLUS User's Manual (MPU-Specific Edition).
Details of memory mapping settings are described on this manual. Please refer to the microVIEW-PLUS User's Manual (MPU-Specific Edition) for other contents.

You are not allowed to set up software break for flash memory in the initial state. In case you try to set up software break for flash memory in the disabled status, it results in "ICE Error No. 8c4: Set Software Break Verify Error".

To enable software break setting for flash memory, select the **Enable** checkbox of S/W Break in Flash Memory on the Others tab of the MPU-Specific Settings dialog box.



7 Notes & Points

7.1 For STM32F2/STM32F4

7.1.1 If the Debugger behavior is Slow when using a Flash Software Break

If 8bitx1 is set for the mapping, it will take 20 seconds for executing a flash software break.

However, you can make the Flash-Rom writing faster depending on the MPU power-supply voltage (VDD) level of the user system environment.

For details, see the following table.

Power-supply voltage (VDD)	Mapping setting Memory I/F Type	Flash definition file (.frd) exp_param3 set value
1.8V to 2.1V	8bit×1	0x4FFFFF0C
2.1V to 2.7V	8bit×1	0x4FFFFF0C
	16bit×1	0x5FFFFF0C
2.7V to 3.6V	8bit×1	0x4FFFFF0C
	16bit×1	0x5FFFFF0C
	32bit×1	0x6FFFFF0C

* The default value of flash definition file (.frd) is 8bit×1 (0x4FFFFF0C).

If the voltage conditions are unknown, please use it with the default value.

Speed of downloading and flash software breaking

8bit×1	16bit×1	32bit×1
Slow	→	Fast

If you change the Memory I/F Type on the Set Mapping dialog box, make sure to change the set value of exp_param3 of the flash definition file (.frd).

After the changing, reconfigure the memory mapping in accordance with Section 4.1 “Setting up Flash Memory Mapping”.

7.1.2 For When a Time-out Error occurs

The following errors occur if the combinations of the setting of flash definition file (.frd) and the Memory I/F Type on the Set mapping dialog box are not correct.

“ICE Message No.1e4a: Time-out occurred when downloading a flash memory.”

“ICE Message No.1e48: Time-out occurred when checking a flash memory status.”

In case an error occurred, check the set value of exp_param3 of the flash definition file and the Memory I/F Type of mapping by reference to the table on the Section 7.1.1.
If you changed the setting of flash definition file, make sure to erase the mapping of flash memory on the Set Mapping dialog box.